APPLICATION NOTE

TEA1210TS High efficiency, high current DC/DC Converter Version 1.0 AN99010

Philips
Semiconductors

PHILIPS

Abstract

This Application Note provides simple guidelines for creating a high efficiency DC/DC conversion function using the TEA1210TS. This document contains three design examples. By adapting the starting conditions the examples can be used to successfully design any application. The appendices contain additional information, such as DC/DC converter theory and lists of manufacturers.

APPLICATION NOTE

TEA1210TS
High efficiency, high current DC/DC Converter

Version 1.0

AN99010

Author:

Arjan van Wijk
Design & Application Consumer Systems Nijmegen
The Netherlands

Keywords

Portable Products
DC/DC Conversion
High Efficiency
TEA1210TS
Up Converter
Down Converter
Dual Current Limit
Cellular Phones
GSM
PDA

November 1999

Summary

The main section of this report contains three design examples, i.e. two Up converters (5.0 V / 650 mA; 4.8 V / 2 A PA supply in GSM phone) and one Down converter (2 V / 1 A). The one example that resembles your application most may be used to create a successful design. Simply adapt the starting conditions and repeat the calculations. Some hints on PCB design are included in this section as well.

The appendices provide basic information about operation of DC/DC converters with inductors and specific formulas for the TEA1210TS are presented. The final appendix contains details on manufacturers of external components.

DC/DC converters are sometimes feared for their 'switching noise'. The TEA1210TS has already proven in many applications that with some attention to the design the side effects of 'switching noise' can be minimised easily.

To test whether the TEA1210TS suits your application several free Evaluation Kits with User Manuals are available.

1. INTRODUCTION

This document gives insight into application of the TEA1210TS DC/DC Converter. One of the three reference designs presented could serve as a fine starting point for your specific design. For more detailed information about TEA1210TS operation and formulas, it is recommended to read the TEA1210TS data sheet or the TEA1207T Application Note AN99007.

This introductory chapter describes the contents of this Application Note and the purpose of each chapter.

The next three sections include reference designs. For your particular application study the example that corresponds with your situation. Simply replace the starting conditions from the example by your own application's values and repeat the calculations.

Chapter 2, "1ST Design example: 5 V / 0.65 A Up converter", covers the design of a 5 V Up converter. It supplies continuous load currents up to 650 mA from a single Li-Ion cell. This chapter takes just two pages.

Chapter 3, "2ND Design example: Up converter to supply 4.8 V PA in GSM phone", explains the design of a 4.8 V Up converter operating on two NiCd/NiMH cells. This design is intended to supply 2 A pulsed load currents to the PA in a GSM phone. Since this example includes some extra figures the chapter takes five pages.

Chapter 4, "3RD Design example: 2 V / 1 A Down converter", covers the design of a 2 V Down converter. The power from three Alkaline cells is converted to supply 1 A continuous load current. This chapter also takes just two pages.

Chapter 5, "PCB design", is merely one page of guidelines. With some attention to PCB design the side effects of 'switching noise' can easily be minimised. Covered topics are component placement, routing and grounding techniques.

In APPENDIX 1 and APPENDIX 2 the basic operation of a DC/DC converter is just briefly clarified. As the TEA1210TS can be configured for Up or Down conversion, both conversion methods are highlighted. For calculations, the TEA1210TS formulas are also presented in these appendices. These formulas are arranged on a single page to form a convenient reference table. More details of the exact operation of DC/DC converters can readily be found in electronic reference books.

Obviously, you will need a list of preferred external components. APPENDIX 3, therefore, contains tables with manufacturers and their Internet addresses. You can download their latest product specifications yourself.

To test whether the TEA1210TS suits your application several free Evaluation Kits with User Manuals are available. You may choose from two mini boards: a single current limit 3.6 V Up converter, or a 2 V Down converter. Additionally, another 3.6 V Up converter board is available for evaluation of the dual current limit feature.

If – after reading this application note – you have any questions or comments feel free to contact your local Philips representative.

2. 1ST DESIGN EXAMPLE: 5 V / 0.65 A UP CONVERTER

This first example covers the design of a 5 V Up converter. It supplies continuous load currents up to 650 mA from a single Li-Ion cell.

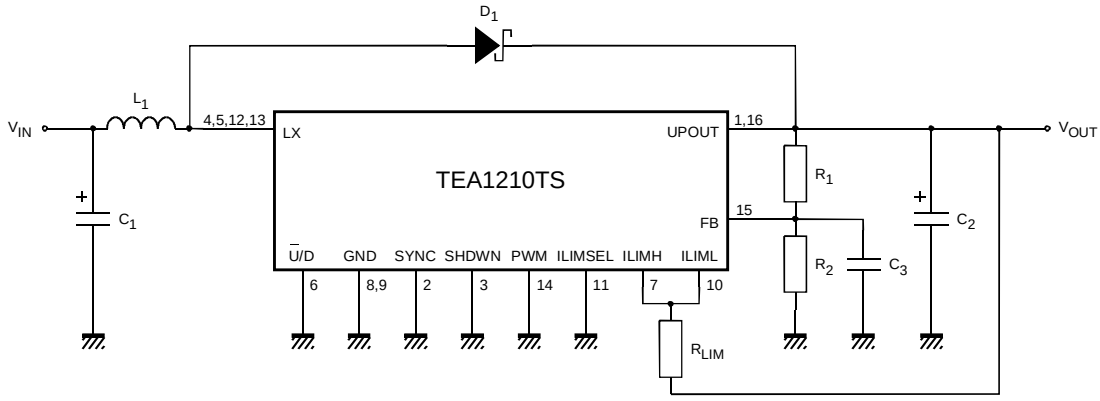


Fig. 1 Application diagram for an Up converter.

Supposed conditions

- Input voltage range: 1 Li-Ion cell, V_{IN} = 2.7…4.2 V
- Typical output voltage: $V_{OUT,TYP}$ = 5.0 V
- Output voltage ripple due to ESR: Ripple = 100 mV_{PP}
- Load current range: I_{LOAD} = 0…650 mA
- Running on internal clock; Shut-down mode not used; automatic PFM/PWM selection; no current limiting.

Characteristics TEA1210TS

- Feedback voltage level: V_{fb} = 1.25 V
- Minimum PWM switching frequency: $f_{SW,PWM,MIN}$ = 480 kHz

Design calculations – worst case scenario

- Feedback resistors R_1 and R_2

$$R_1 = 50k\Omega \cdot \frac{V_{OUT,TYP}}{V_{fb}} = 50k\Omega \cdot \frac{5.0V}{1.25V} = 200k\Omega \pm 1\%(SMD)$$

$$R_2 = R_1 \cdot \frac{V_{fb}}{V_{OUT,TYP} - V_{fb}} = 200k\Omega \cdot \frac{1.25V}{5.0V - 1.25V} = 66.5k\Omega \pm 1\%(SMD)$$

- Inductor L_1

$$\delta_{MAX} = 1 - \frac{V_{IN,MIN}}{V_{OUT,TYP}} = 1 - \frac{2.7V}{5.0V} = 46\%$$

$$I_{SAT} \geq I_{PEAK,MAX} = \frac{V_{OUT,TYP} \cdot I_{LOAD,MAX}}{0.85 \cdot V_{IN,MIN}} + \frac{1}{2} \cdot \frac{\delta_{MAX} \cdot V_{IN,MIN}}{f_{SW,PWM,MIN} \cdot L} = \frac{5.0V \cdot 0.65A}{0.85 \cdot 2.7V} + \frac{1}{2} \cdot \frac{46\% \cdot 2.7V}{480kHz \cdot L} =$$

$$= 1.41A + \frac{1.29}{L(\mu H)}. \; For\ L = 6.8\mu H, I_{SAT} \geq 1.6A.$$

When searching for a 6.8 µH inductor with at least I_{SAT} = 1.6 A, the SLF7032T-6R8M1R6 from TDK was found to fit this particular application. It represents a DC resistance of 47 mΩ and I_{SAT} = 1.6 A.

- Current limit level
  Since the current limit feature is not used explicitly, the current limit should be set at a high level, just for protection.

  $$I_{LIM} \geq \frac{I_{SAT}}{0.75} = \frac{1.6A}{0.75} = 2.13A$$

- Current limit resistor R_{LIM}

  $$R_{LIM} \leq \frac{346}{I_{LIM} - 0.05} = \frac{346}{2.13 - 0.05} = 165\Omega \pm 5\% (SMD)$$

- Output capacitor C_2
  The starting point for choosing the output capacitor is the maximum output voltage ripple that you allow. This ripple is mainly caused by the output capacitor's ESR.

  $$Ripple = I_{PEAK,MAX} \cdot ESR = \left(1.41A + \frac{1.29}{6.8}\right) \cdot ESR = 1.6A \cdot ESR$$

  In this example, we allow about 100 mV_{PP} ripple.

  $$ESR \leq \frac{100mV}{1.6A} = 62.5m\Omega$$

  TPSD107M010R0065 from AVX – 100 µF/10 V in D-case – features 65 mΩ ESR and 1.5 A RMS current.

- Input capacitor C_1
  The input capacitor's ESR must be lower than the internal resistance of the power supply. It should also be within the range of the inductor's DCR, output capacitor's ESR and the R_{dsON} of the TEA1210TS power switches. In this example, that range is about 55…65 mΩ. The same capacitor as mentioned above may be used here.

- Feedback capacitor C_3
  To remove switching noise from the feedback voltage, a ceramic capacitor – having a maximum value of 33 pF – is recommended.

- Schottky diode D_1
  For almost any application, the Philips PRLL5819 is a good choice.

Remark:
In case you want to limit the output power by using the current limit feature explicitly, then you should use:

$$I_{SAT} \geq 1.27 \cdot I_{PEAK,MAX}$$

$$I_{LIM} \geq \frac{I_{PEAK,MAX}}{0.88}$$

3. 2ND DESIGN EXAMPLE: UP CONVERTER TO SUPPLY 4.8 V PA IN GSM PHONE

The second example is based on a GSM load pattern, with a pulsed load of 2 A. If any DC/DC converter had to deliver all power by itself, a big inductor would be required for this application. The demanded saturation current would be higher than 8 A, which is something you do not want! An alternative solution for this application is shown in Fig. 2. This small application reduces size of DC/DC Converter and inductor at the cost of a reservoir capacitor and large output voltage ripple. The TEA1210TS dual current limit feature has been designed especially for this pulsed load.

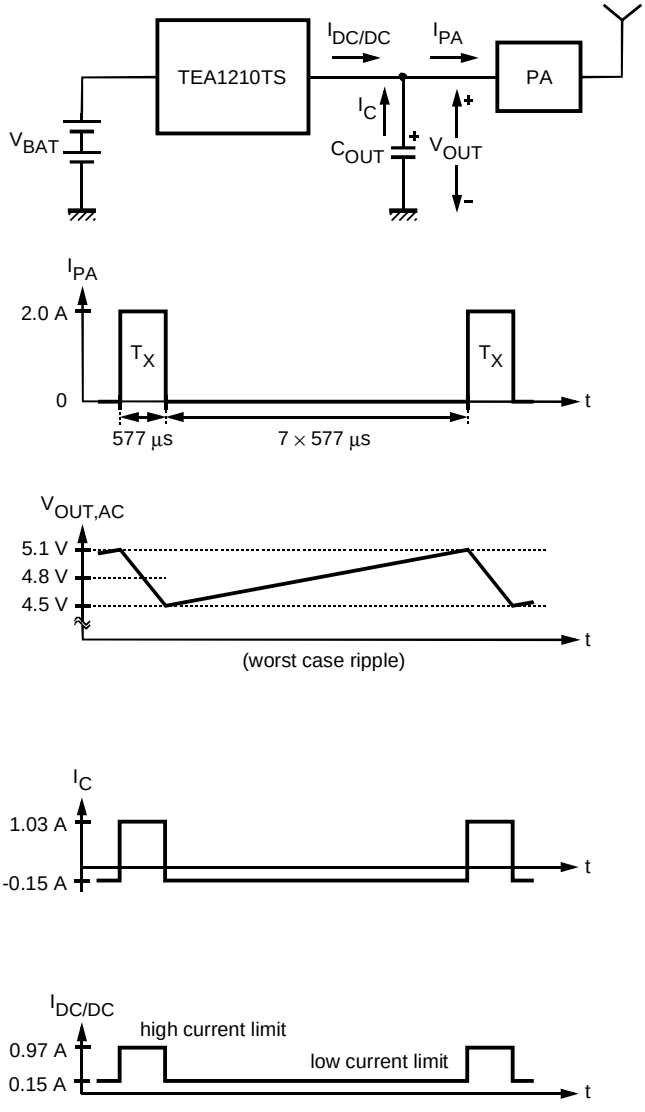


Fig. 2 Block diagram and wave forms for 4.8 V PA supply in GSM phone.

During transmission bursts (T_x), the output capacitor supplies most of the energy to the 4.8 V Power Amplifier (PA). As a result the output capacitor discharges during T_x. The TEA1210TS supplies the required extra energy with a high current limit level.

$I_{PA} = I_C + I_{DC/DC} = 2.0\,A$, during T_x

During the $7 \times T_x$ time between the bursts, TEA1210TS recharges the output capacitor very efficiently by using a low current limit level. Obviously, the capacitor must be fully charged before the next T_x.

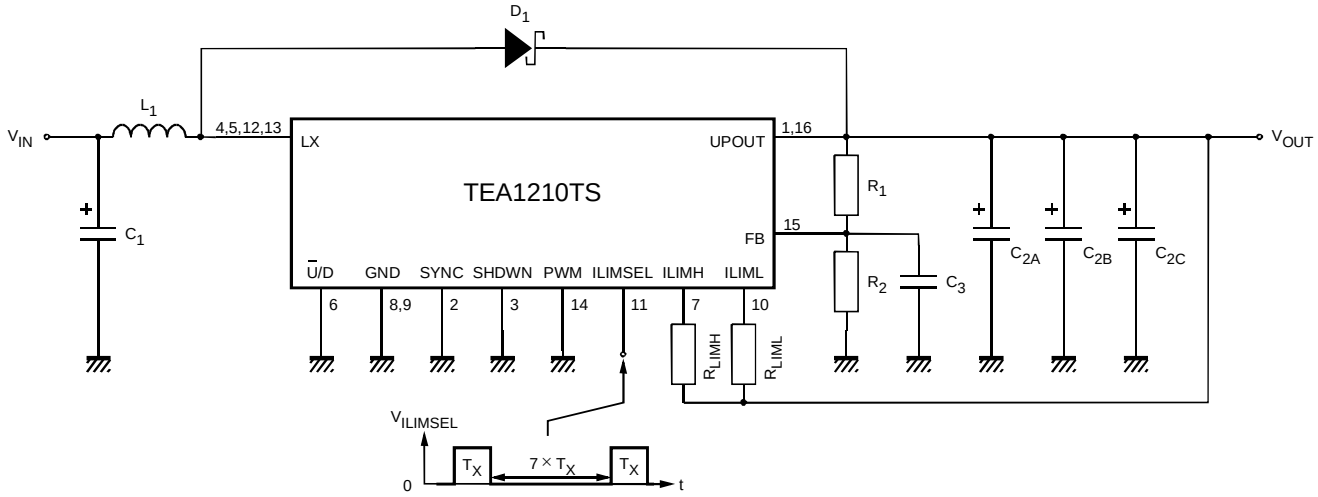


Fig. 3 Application diagram for PA supply in GSM phone.

Supposed conditions

- 2 NiCD/NiMH cells: V_{BAT} = 1.8…2.6 V, $I_{BAT,MAX}$ = 2.0 A, R_{BAT} = 100 mΩ
- Average output voltage during T_x: $V_{OUT,AVG}$ = 4.8 V
- Maximum output voltage just before T_x: $V_{OUT,MAX}$ = 5.1 V
- Minimum output voltage just after T_x: $V_{OUT,MIN}$ = 4.5 V
- Load current range: I_{LOAD} = 0…2.0 A
- Output capacitors: maximum PCB space for three D-cases, e.g. $3 \times 330\ \mu F = 990\ \mu F$
- Target inductor series: SLF12565T from TDK.
- Running on internal clock; Shut-down mode not used; automatic PFM/PWM selection.
- Dual current limiting feature used: high current limit level during T_x, low level during $7 \times T_x$.

Characteristics TEA1210TS

- Feedback voltage level: V_{fb} = 1.25 V
- Minimum PWM switching frequency: $f_{SW,PWM,MIN}$ = 480 kHz

Design calculations – worst case scenario

- Feedback resistors R_1 and R_2
  Since the output capacitor must be charged to 5.1 V, this must be the target output voltage. Not the 4.8 V.

$$R_1 = 50k\Omega \cdot \frac{V_{OUT,TYP}}{V_{fb}} = 50k\Omega \cdot \frac{5.1V}{1.25V} = 205k\Omega \pm 1\%(SMD)$$

$$R_2 = R_1 \cdot \frac{V_{fb}}{V_{OUT,TYP} - V_{fb}} = 205k\Omega \cdot \frac{1.25V}{5.1V - 1.25V} = 66.5k\Omega \pm 1\%(SMD)$$

- Minimum input voltage for DC/DC converter

$$V_{IN,MIN} = V_{BAT,MIN} - \left(I_{BAT,MAX} \cdot R_{BAT}\right) = 1.8V - \left(2.0A \cdot 0.1\Omega\right) = 1.6V$$

- Maximum load current during T_x

  From this point onwards we will focus on interval T_x.

  Before we can select the inductor, we must determine the maximum load current for the TEA1210TS. In order to do this we need to know the maximum capacitor current.

$$I_C = \frac{C_{OUT} \cdot \left(V_{OUT,MAX} - V_{OUT,MIN}\right)}{T_X} = \frac{990\mu F \cdot \left(5.1V - 4.5V\right)}{577\mu s} = 1.03A$$

$$I_{LOAD,MAX} = I_{DC/DC} = I_{PA} - I_C = 2.0A - 1.03A = 0.97A$$

- High current limit during T_x

  For the GSM phones produced, each TEA1210TS must be able to deliver the maximum load current – even when the actual current limit appears to be 12% below the programmed target, which is still within specification limits.

  This means that 88% of I_{LIMH} should be equal to the maximum possible inductor peak current $I_{PEAK,MAX}$.

$$I_{LIMH} = \frac{I_{PEAK,MAX}}{0.88} = 1.14 \cdot I_{PEAK,MAX}$$

  We will use this equation to select the inductor.

- Inductor L_1

  During T_x the average output voltage is 4.8 V, so the average duty cycle will be:

$$\delta_{AVG} = 1 - \frac{V_{IN,MIN}}{V_{OUT,AVG}} = 1 - \frac{1.6V}{4.8V} = 67\%$$

$$I_{PEAK,MAX} = \frac{V_{OUT,AVG} \cdot I_{LOAD,MAX}}{0.75 \cdot V_{IN,MIN}} + \frac{1}{2} \cdot \frac{\delta_{AVG} \cdot V_{IN,MIN}}{f_{SW,PWM,MIN} \cdot L} = \frac{4.8V \cdot 0.97A}{0.75 \cdot 1.6V} + \frac{1}{2} \cdot \frac{67\% \cdot 1.6V}{480kHz \cdot L} =$$

$$= 3.88A + \frac{1.12}{L(\mu H)}$$

$$I_{LIMH} = 1.14 \cdot I_{PEAK,MAX} = 1.14 \cdot \left(3.88A + \frac{1.12}{L(\mu H)}\right) = 4.42A + \frac{1.28}{L(\mu H)}$$

  It now appears as if any inductor may be selected. Just substitute the inductance in the equation above and you will have your target I_{LIMH}. But remember the selected inductor may never saturate – not even when the actual current limit appears to be 12% above programmed target, which is also within specification limits. In formula:

$$I_{SAT} \geq 1.12 \cdot I_{LIMH} = 4.95A + \frac{1.43}{L(\mu H)}$$

  When checking the SLF12565T series from TDK, the 7 µH inductor – SLF12565T-7R0N5R0 – was found suitable for this particular application. It represents a DC resistance of 177 mΩ and I_{SAT} = 5.0 A, which is very close to the required 5.15 A.

- Current limit resistor R_{LIMH}
  Now we can calculate the target current limit I_{LIMH} when we fill in 7 for L (μH)

$$I_{LIMH} = 4.42A + \frac{1.28}{7} = 4.60A$$

$$R_{LIMH} \le \frac{346}{I_{LIMH} - 0.05} = \frac{346}{4.60 - 0.05} = 75\Omega \pm 1\% (SMD)$$

- Load current between transmission bursts T_x
  From this point onwards we will focus on interval between two transmission bursts T_x.
  After each transmission burst T_x, the output capacitors have been discharged by 600 mV at most. The TEA1210TS should recharge them to 5.1 V. Recharging with a low current is much more efficient than recharging with a high current. As the output capacitors should be fully recharged only just before the next T_x, we will set the recharge current – i.e. I_{LOAD} – as small as possible.

$$I_{LOAD} = \frac{C_{OUT} \cdot \left(V_{OUT,MAX} - V_{OUT,MIN}\right)}{7 \cdot T_X} = \frac{990\mu F \cdot \left(5.1V - 4.5V\right)}{7 \cdot 577\mu s} = 0.15A$$

- Low current limit between transmission bursts T_x
  Setting the recharge current is achieved by programming the low current limit I_{LIML}. For low currents the tolerance on the current limit level is 20%. This means that 80% of I_{LIML} should be equal to the inductor peak current I_{PEAK}.

$$I_{LIML} = \frac{I_{PEAK}}{0.80} = 1.25 \cdot I_{PEAK}$$

$$I_{PEAK} = \frac{V_{OUT,AVG} \cdot I_{LOAD}}{0.85 \cdot V_{IN,MIN}} + \frac{1}{2} \cdot \frac{\delta_{AVG} \cdot V_{IN,MIN}}{f_{SW,PWM,MIN} \cdot L} = \frac{4.8V \cdot 0.15A}{0.85 \cdot 1.6V} + \frac{1}{2} \cdot \frac{67\% \cdot 1.6V}{480kHz \cdot L} =$$

$$= 0.53A + \frac{1.12}{L(\mu H)}$$

$$I_{LIML} = 1.25 \cdot I_{PEAK} = 1.25 \cdot \left(0.53A + \frac{1.12}{7}\right) = 0.86A$$

- Current limit resistor R_{LIML}

$$R_{LIML} \le \frac{346}{I_{LIML} - 0.05} = \frac{346}{0.86 - 0.05} = 422\Omega \pm 1\% (SMD)$$

- ILIMSEL-pin control
  Producing the required $I_{DC/DC}$ wave form as shown in Fig. 2 has now become easy. All that is required is a signal with the same shape as I_{PA} and connect it to ILIMSEL (pin 11), see Fig. 3. The specifications for the low level and high level of this signal are:

$$V_{LO} = 0 \ldots 0.4V$$

$$V_{HI} = 55\% \text{ of } V_1 \ldots V_1 + 0.3V, \text{ where } V_1 \text{ is the minimum voltage at the output (pin1), i.e. } 4.5V$$
$$= 2.5 \ldots 4.8V$$

  A digital low on ILIMSEL (pin 11) selects the resistor connected to ILIML (pin 7) – i.e.R_{LIML}. – for current limiting. Where as a digital high selects the resistor connected to ILIMH (pin 10), i.e.R_{LIMH}.
  Note: if the available ILIMSEL-signal in your system is inverted, then you will have to swap R_{LIML} and R_{LIMH}.

- Output capacitors C_{2A}, C_{2B} and C_{2C}
  In this example, there is only PCB space for three D-case, e.g. 3 × 330 µF = 990 µF.
  The TPSD337M010R0150 from AVX fulfils this requirement. The ESR of one single capacitor is 150 mΩ, three in parallel results in 50 mΩ ESR.
  The low frequent output ripple (Fig. 2) is 600 mV_{PP}. During T_X the ripple due to ESR is less:

$$Ripple = I_{PEAK,MAX} \cdot ESR = \left(3.88A + \frac{1.12}{7} \right) \cdot 50m\Omega = 202mV$$

- Input capacitor C_1
  The input capacitor's ESR must be lower than the internal resistance of the power supply. It should also be within the range of the inductor's DCR and the RdsON of the TEA1210TS power switches. In this example, that range is about 55…177 mΩ. TPSD107M010R0065 from AVX – 100 µF/10 V in D-case – features 65 mΩ ESR and 1.5 A RMS current.
- Feedback capacitor C_3
  To remove switching noise from the feedback voltage, a ceramic capacitor – having a maximum value of 33 pF – is recommended.
- Schottky diode D_1
  For almost any application, the Philips PRLL5819 is a good choice.

The benefits of this solution are:

1. maintaining high efficiency figures
2. higher output power capability than TEA1210TS has by itself
3. the DC/DC converter can be small and cheap (hence the TEA1210TS is used)
4. inductor is smaller and thus cheaper

This approach saves considerable costs on the DC/DC converter and inductor, but it requires additional capacitance to serve as an energy reservoir for peak power. Fortunately, capacitor manufacturers are releasing ever greater capacitance in ever smaller packages, so even a total output capacitance of 1000 µF to 2000 µF will have acceptable dimensions.

4. 3RD DESIGN EXAMPLE: 2 V / 1 A DOWN CONVERTER

The third example is a 2 V Down converter for 1 A maximum continuous load current.

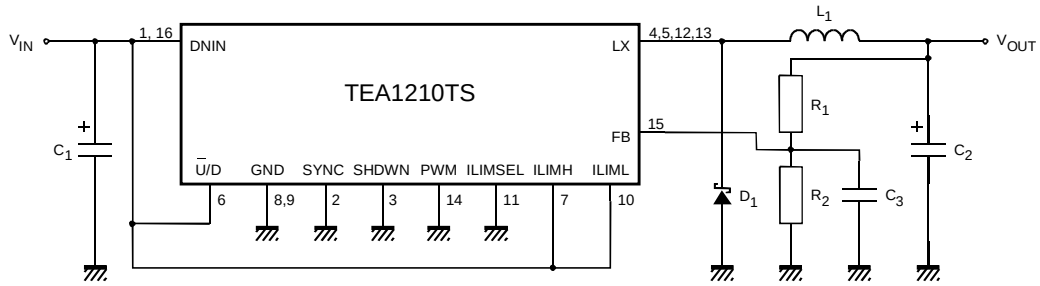


Fig. 4 Application diagram for a 2 V / 1 A Down converter.

Supposed conditions

- Input voltage range: 3 Alkaline cells, V_{IN} = 2.7…4.8 V
- Typical output voltage: $V_{OUT,TYP}$ = 2.0 V
- Output voltage ripple due to ESR: Ripple < 100 mV_{PP}
- Load current range: I_{LOAD} = 0…1 A
- Running on internal clock; Shut-down mode not used; automatic PFM/PWM selection.

Characteristics TEA1210TS

- Feedback voltage level: V_{fb} = 1.25 V
- Minimum PWM switching frequency: $f_{SW,PWM,MIN}$ = 480 kHz

Design calculations – worst case scenario

- Feedback resistors R_1 and R_2

$$R_1 = 50k\Omega \cdot \frac{V_{OUT,TYP}}{V_{fb}} = 50k\Omega \cdot \frac{2.0V}{1.25V} = 80.6k\Omega \pm 1\%(SMD)$$

$$R_2 = R_1 \cdot \frac{V_{fb}}{V_{OUT,TYP} - V_{fb}} = 80.6k\Omega \cdot \frac{1.25V}{2.0V - 1.25V} = 133k\Omega \pm 1\%(SMD)$$

- Inductor L_1

$$\delta_{MIN} = \frac{V_{OUT,TYP}}{V_{IN,MAX}} = \frac{2.0V}{4.8V} = 41\%$$

$$I_{SAT} \geq I_{PEAK,MAX} = I_{LOAD,MAX} + \frac{1}{2} \cdot \frac{\delta_{MIN} \cdot (V_{IN,MAX} - V_{OUT,TYP})}{f_{SW,PWM,MIN} \cdot L} = 1A + \frac{1}{2} \cdot \frac{41\% \cdot (4.8V - 2.0V)}{480kHz \cdot L} =$$

$$= 1A + \frac{1.20}{L(\mu H)}.\ For\ L = 10\mu H,\ I_{SAT} \geq 1.12A.$$

When searching for a 6.8 µH inductor with about I_{SAT} = 1.12 A, the DO1608C-103 from Coilcraft was found suitable for this particular application. It represents a DC resistance of 160 mΩ and I_{SAT} = 1.1 A.

- Current limit level
  The current limit is fixed internally at approximately 4.8 A.
- Output capacitor C_2
  The starting point for choosing the output capacitor is the maximum output voltage ripple that you allow. This ripple is mainly caused by the output capacitor's ESR.

  $$Ripple = I_{PEAK,MAX} \cdot ESR = \left(1A + \frac{1.20}{10}\right) \cdot ESR = 1.12A \cdot ESR$$

  In this example, we allow 100 mV_{PP} ripple at most.

  $$ESR \leq \frac{100mV}{1.12A} = 89m\Omega$$

  594D227X06R3C2T by Sprague – 220 μF/6.3 V in C-case – features 80 mΩ ESR and 1.11 A RMS current.
- Input capacitor C_1
  The input capacitor's ESR must be lower than the internal resistance of the power supply. It should also be within the range of the inductor's DCR, output capacitor's ESR and the R_{dsON} of the TEA1210TS power switches. In this example, that range is about 55…160 mΩ. The same capacitor as mentioned above may be used here.
- Feedback capacitor C_3
  To remove switching noise from the feedback voltage, a ceramic capacitor – having a maximum value of 33 pF – is recommended.
- Schottky diode D_1
  For almost any application, the Philips PRLL5819 is a good choice.

5. PCB DESIGN

DC/DC converters are sometimes feared for their 'switching noise'. The TEA1210TS has already proven in many applications that with some attention to PCB design the side effects of 'switching noise' can easily be reduced to meet emission norms. Printed circuit board (PCB) layout is critical for quiet operation. PCB design starts with identifying the most noisy current loops. Alternating, high currents are flowing through these loops at high frequency. Minimise loop area by correct component placing and using short and wide copper traces. Therefore, the most important rule is:

- Up conversion: place output capacitor C_1 close to UPOUT/DNIN (pins 1 and 16) and GND (pins 8 and 9)
- Down conversion: place input capacitor C_1 close to UPOUT/DNIN (pins 1 and 16) and GND (pins 8 and 9)

Finally, star ground and a ground plane are recommended, see below.

Additional guidelines:

1. inductor current loop area is minimised by placing inductor L1, capacitors C1 and C2 and Schottky diode D1 as close to the TEA1210TS as possible.
2. the preferred method is to place L1, C1, C2 and D1 on PCB top side, TEA1210TS, resistors and capacitor C3 should be located on the bottom side – another option is to put all components on one single PCB side
3. connect the two GND-pins (pins 8 and 9) to each other
4. connect the two UPOUT/DNIN-pins (pins 1 and 16) to each other
5. connect the four LX-pins (pins 4, 5, 12 and 13) to each other
6. position the negative terminals of C_1 and C_2 as close to each other as possible
7. insert L_1 between LX (pins 4, 5, 12 and 13) and the positive terminals of the nearest capacitor, which is C_1 for Up conversion and C_2 for Down conversion
8. place the cathode of D_1 close to the positive terminal of C_2
9. connect the positive supply rail – e.g. from battery – to the positive terminal of C_1
10. start the DC/DC output trace from the positive terminal of C_2
11. connect supply GND to the point where the negative terminals of C_1 and C_2 meet: i.e. star ground
12. start the output GND from this star ground
13. use short and wide traces to connect the TEA1210TS, L_1, C_1, C_2 and D_1;
    traces from TEA1210TS to the resistors and capacitor C_3 may be narrow, since currents are low
14. with components on top side and bottom side, use so-called vias to route from top to bottom;
    the more vias in parallel, the lower the total resistance!
15. keep noisy signals – i.e. their copper traces – away from FB (pin 15)
16. use a ground plane (copper area) directly underneath TEA1210TS, connected to GND (pins 8 and 9);
    with a multilayer PCB, also use a ground plane (ground layer) under the TEA1210TS and its external components: this prevents interplane coupling

APPENDIX 1 UP CONVERSION THEORY

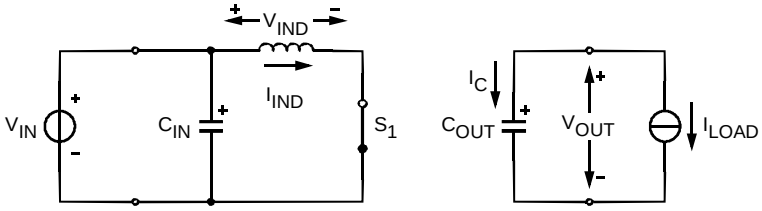


Fig. 5 Equivalent diagram of the Up converter, when switch S_1 is closed

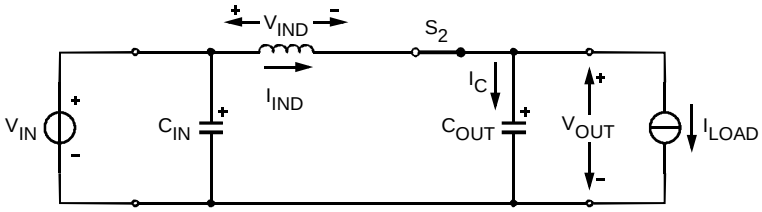
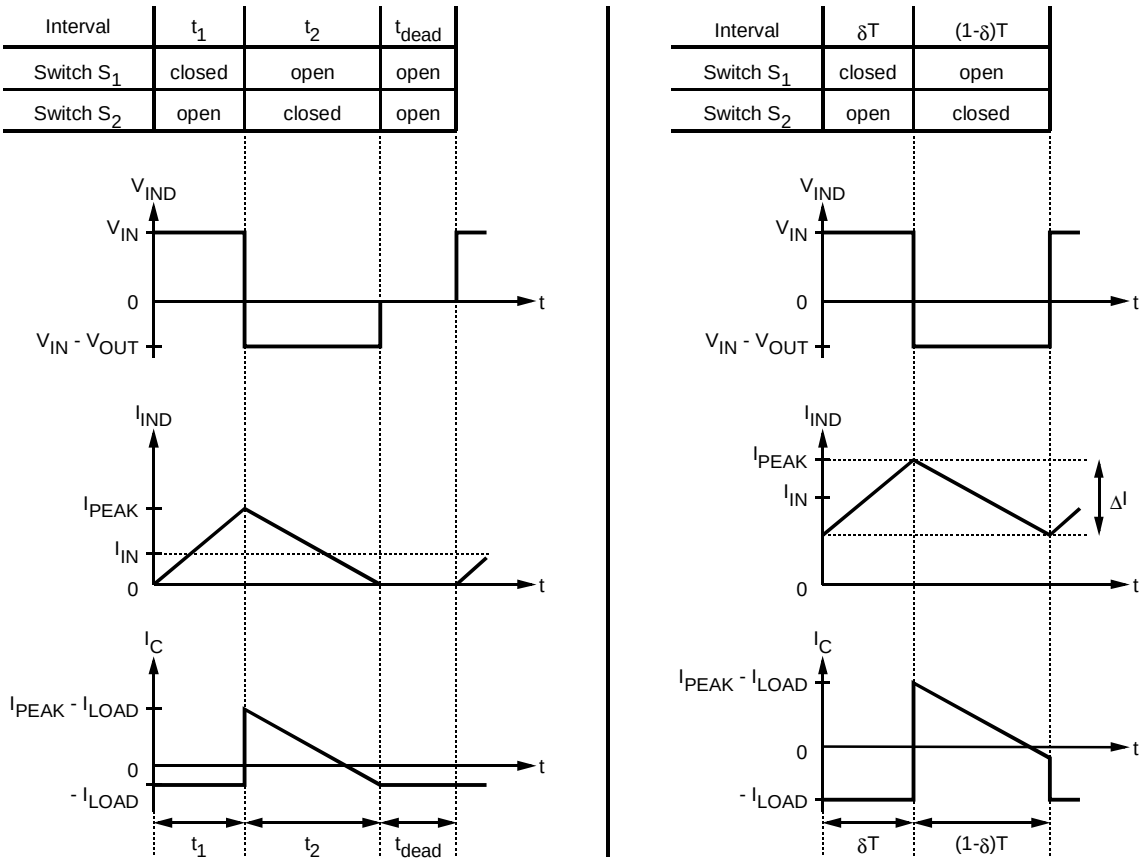


Fig. 6 Equivalent diagram of the Up converter, when switch S_2 is closed



a) PFM b) PWM

Fig. 7 Simplified wave forms for the Up converter

TEA1210TS general formulas		
Output power	$P_{OUT} = V_{OUT} \cdot I_{LOAD}$	(1)
Input power	$P_{IN} = V_{IN} \cdot I_{IN}$	(2)
Efficiency	$\eta = \frac{P_{OUT}}{P_{IN}}$, so $P_{OUT} = P_{IN}$ in case of $\eta = 100\%$	(3)
Internal clock frequency	$f_{CLOCK} = 13.2\ \text{MHz} \pm 20\%$	(4)
External sync. frequency	$9\ \text{MHz} \leq f_{SYNC} \leq 20\ \text{MHz}$	(5)

TEA1210TS formulas for Up conversion in PFM		
First interval	$\frac{7}{f_{CLOCK}} \leq t_1 \leq \frac{21}{f_{CLOCK}}$, or $\frac{7}{f_{SYNC}} \leq t_1 \leq \frac{21}{f_{SYNC}}$	(6)
Second interval	$t_2 = t_1 \cdot \frac{V_{IN}}{V_{OUT} - V_{IN}}$	(7)
Third interval	t_{dead} is undefined	
Inductor peak current	$I_{PEAK} = t_1 \cdot \frac{V_{IN}}{L}$	(8)
Input current	$I_{IN} = I_{IND,AVG}$	(9)
Average inductor current	$I_{IND,AVG} = \frac{1}{2} \cdot I_{PEAK} \cdot \frac{t_1 + t_2}{t_1 + t_2 + t_{dead}}$	(10)
Maximum possible load current	$I_{LOAD,MAX} = \eta \cdot I_{IN,MAX} \cdot \frac{V_{IN}}{V_{OUT}} = \eta \cdot \frac{1}{2} \cdot I_{PEAK} \cdot \frac{V_{IN}}{V_{OUT}}$	(11)

TEA1210TS formulas for Up conversion in PWM		
Switching frequency	$f_{SW,PWM} = \frac{f_{CLOCK}}{22} = \frac{1}{T}$, or $f_{SW,PWM} = \frac{f_{SYNC}}{22} = \frac{1}{T}$	(12)
Duty-cycle	$\delta = 1 - \frac{V_{IN}}{V_{OUT}}$	(13)
Inductor peak-to-peak current	$\Delta I = \delta T \cdot \frac{V_{IN}}{L} = \frac{\delta \cdot V_{IN}}{f_{SW,PWM} \cdot L}$	(14)
Input current	$I_{IN} = \frac{1}{\eta} \cdot I_{LOAD} \cdot \frac{V_{OUT}}{V_{IN}}$	(15)
Average inductor current	$I_{IND,AVG} = I_{IN}$	(16)
Inductor peak current	$I_{PEAK} = I_{IND,AVG} + \frac{1}{2} \cdot \Delta I$	(17)
Minimum possible load current	$I_{LOAD,MIN} = \eta \cdot I_{IN,MIN} \cdot \frac{V_{IN}}{V_{OUT}} = \eta \cdot \frac{1}{2} \cdot \Delta I \cdot \frac{V_{IN}}{V_{OUT}}$	(18)

APPENDIX 2 DOWN CONVERSION THEORY

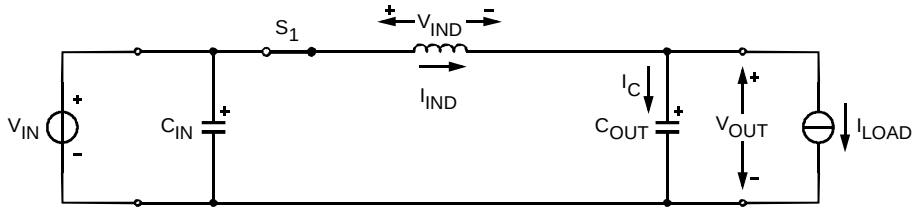


Fig. 8 Equivalent diagram of the Down converter, when switch S_1 is closed

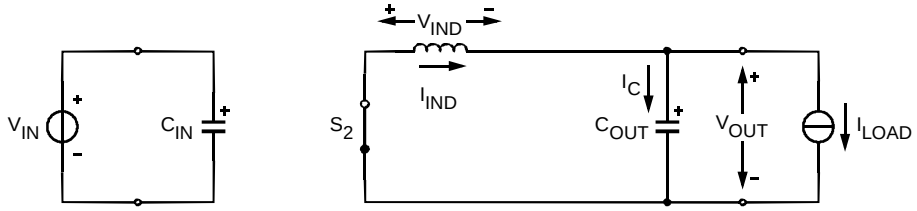
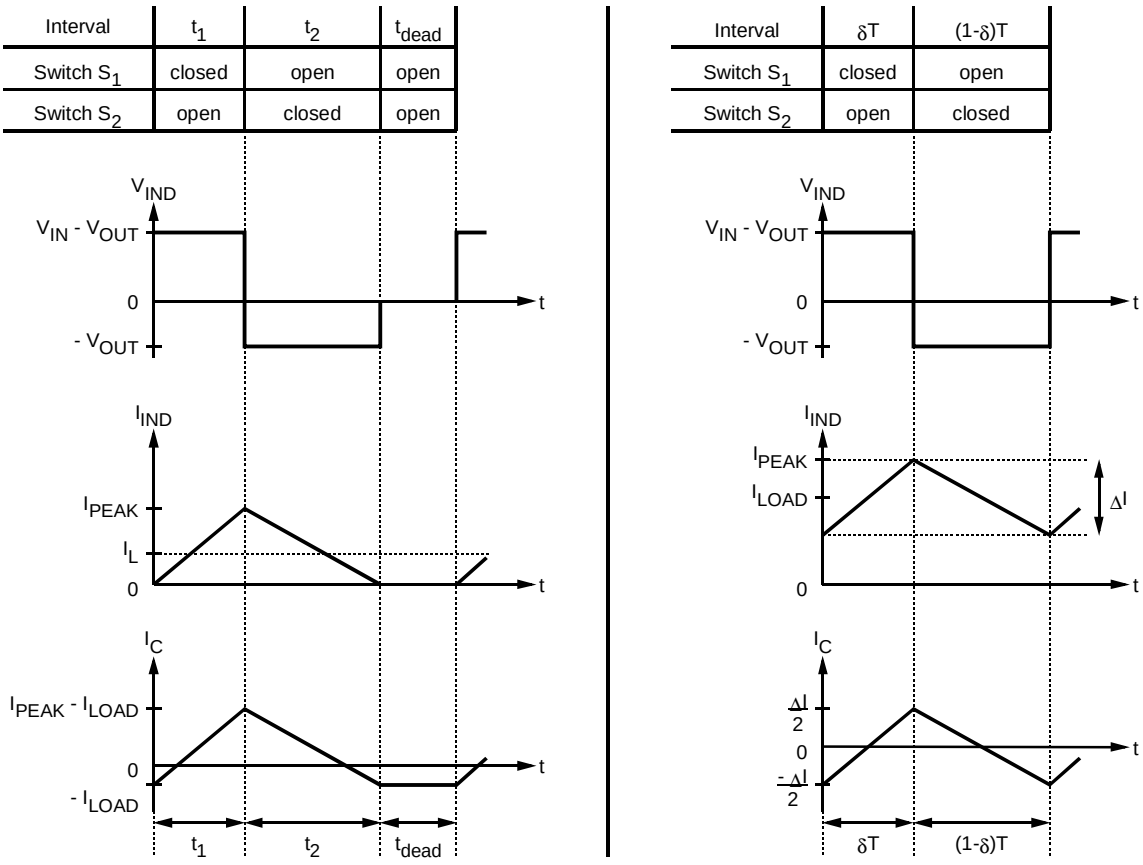


Fig. 9 Equivalent diagram of the Down converter, when switch S_2 is closed



a) PFM b) PWM

Fig. 10 Simplified wave forms for the Down converter

TEA1210TS general formulas		
Output power	$P_{OUT} = V_{OUT} \cdot I_{LOAD}$	(1)
Input power	$P_{IN} = V_{IN} \cdot I_{IN}$	(2)
Efficiency	$\eta = \frac{P_{OUT}}{P_{IN}}$, so $P_{OUT} = P_{IN}$ in case of $\eta = 100\%$	(3)
Internal clock frequency	$f_{CLOCK} = 13.2\ \text{MHz} \pm 20\%$	(4)
External sync. frequency	$9\ \text{MHz} \leq f_{SYNC} \leq 20\ \text{MHz}$	(5)

TEA1210TS formulas for Down conversion in PFM		
First interval	$\frac{7}{f_{CLOCK}} \leq t_1 \leq \frac{23}{f_{CLOCK}}$, or $\frac{7}{f_{SYNC}} \leq t_1 \leq \frac{23}{f_{SYNC}}$	(19)
Second interval	$t_2 = t_1 \cdot \frac{V_{IN} - V_{OUT}}{V_{OUT}}$	(20)
Third interval	t_{dead} is undefined	
Inductor peak current	$I_{PEAK} = t_1 \cdot \frac{V_{IN} - V_{OUT}}{L}$	(21)
Input current	$I_{IN} = \frac{1}{\eta} \cdot I_{IND,AVG} \cdot \frac{V_{OUT}}{V_{IN}}$	(22)
Average inductor current	$I_{IND,AVG} = I_{LOAD}$	(23)
Maximum possible load current	$I_{LOAD,MAX} = \frac{1}{2} \cdot I_{PEAK}$	(24)

TEA1210TS formulas for Down conversion in PWM		
Switching frequency	$f_{SW,PWM} = \frac{f_{CLOCK}}{22} = \frac{1}{T}$, or $f_{SW,PWM} = \frac{f_{SYNC}}{22} = \frac{1}{T}$	(12)
Duty-cycle	$\delta = \frac{V_{OUT}}{V_{IN}}$	(25)
Inductor peak-to-peak current	$\Delta I = \delta T \cdot \frac{V_{IN} - V_{OUT}}{L} = \frac{\delta \cdot (V_{IN} - V_{OUT})}{f_{SW,PWM} \cdot L}$	(26)
Input current	$I_{IN} = \frac{1}{\eta} \cdot I_{LOAD} \cdot \frac{V_{OUT}}{V_{IN}}$	(15)
Average inductor current	$I_{IND,AVG} = I_{LOAD}$	(23)
Inductor peak current	$I_{PEAK} = I_{IND,AVG} + \frac{1}{2} \cdot \Delta I$	(17)
Minimum possible load current	$I_{LOAD,MIN} = \frac{1}{2} \cdot \Delta I$	(27)

APPENDIX 3 LIST OF MANUFACTURERS

Inductor manufacturer	Series (Surface Mount)	Internet
Coilcraft	DO1608, DS1608, DT1608 DO3308 DO3316, DS3316, DT3316	www.coilcraft.com
Coiltronics	CTX, TP, UP	www.coiltronics.com
TDK	SLF	www.tdk.co.jp
TOKO	3DF, D62F, D62C, D73LF, D73LC, D73F, D73C, D73CT	www.toko.co.jp

Capacitor manufacturer	Series (Surface Mount)	Internet
AVX	TPS	www.avxcorp.com
Kemet	T494, T495	www.kemet.com
muRata	GRM42, GRM200	www.murata.co.jp
Sanyo	TPA, TPB (POSCAP)	www.sanyo.co.jp
Vishay/Sprague	593D, 594D, 595D	www.vishay.com

Schottky diode manufacturer	Series (Surface Mount)	Internet
Motorola	MBR0540T1, MBRM120LT3	www.mot.com
Philips	PRLL5817, 5818, 5819	www.philips.com